U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/85	
Application Number 10/791,501	Filing Date March 1, 2004	Examiner James K. Trujillo	Art Unit 2116
Invention Title RUNTIME CONFIGURABLE ARITHMETIC AND LOGIC CELL		Inventor Martin VORBACH et al.	

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on:
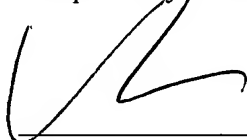
Date: August 28, 2007

Signature: _____
Michelle M. Carniaux (Reg. No. 36,098)

SIR:

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 35 U.S.C. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby brings the following references to the attention of the Examiner. These references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

2. The filing of this Information Disclosure Statement and the enclosed PTO 1449 shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. §1.56(b).

3. A copy of each patent, publication or other information listed on the modified PTO 1449 is enclosed, except for United States patent references or where indicated on the list of references (Form 1449).

4. It is believed that no fees are due in connection with this Information Disclosure Statement. However, should any fees be due, the Commissioner is authorized to charge Deposit Account No. 11-0600 for such fees. A duplicate of this communication is enclosed for charging purposes.
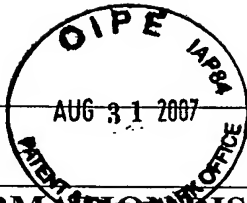
Respectfully submitted,

Dated: August 28, 2007
CUSTOMER NUMBER 26646

By: Michelle M. Carniaux (Reg. No. 36,098)
KENYON & KENYON LLP
One Broadway
New York, N.Y. 10004
(212) 425-7200 (telephone)
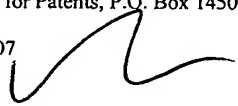(212) 425-5288 (facsimile)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
INFORMATION DISCLOSURE STATEMENT	Docket Number: **2885/85**		
Application Number **10/791,501**	Filing Date **March 1, 2004**	Examiner **James K. Trujillo**	Art Unit **2116**
Invention Title **RUNTIME CONFIGURABLE ARITHMETIC AND LOGIC CELL**		Inventor **Martin VORBACH et al.**	

Address to:

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on:

Date: August 28, 2007

Signature: _____
    Michelle M. Carniaux (Reg. No. 36,098)

SIR:

1.   In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 35 U.S.C. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby brings the following references to the attention of the Examiner. These references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

2.   The filing of this Information Disclosure Statement and the enclosed PTO 1449 shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. §1.56(b).

3.   A copy of each patent, publication or other information listed on the modified PTO 1449 is enclosed, except for United States patent references or where indicated on the list of references (Form 1449).

4.   It is believed that no fees are due in connection with this Information Disclosure Statement. However, should any fees be due, the Commissioner is authorized to charge Deposit Account No. 11-0600 for such fees. A duplicate of this communication is enclosed for charging purposes.
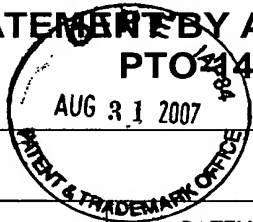
Respectfully submitted,

Dated: August 28, 2007
CUSTOMER NUMBER 26646

By: Michelle M. Carniaux (Reg. No. 36,098)
KENYON & KENYON LLP
One Broadway
New York, N.Y. 10004
(212) 425-7200 (telephone)
(212) 425-5288 (facsimile)

<table>
<tr><td colspan="2"></td><td>Attorney Docket No.
2885/85</td><td>Serial No.
10/791,501</td></tr>
<tr><td colspan="2" rowspan="3">INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO 1449
AUG 31 2007</td><td colspan="2">Applicant(s)
Vorbach et al.</td></tr>
<tr><td>Filing Date
March 1, 2004</td><td>Group Art Unit
2116</td></tr>
</table>

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,233,667	November 11, 1980	Devine et al.			
	4,720,778	January, 1998	Hansen et al.			
	4,918,440	April 17, 1990	Furtek et al.			
	5,361,373	November 1, 1994	Gilson			
	5,392,437	February 21, 1995	Matter et al.			
	5,737,516	April 1998	Circello et al.			
	5,841,973	November 1998	Cooke et al.			
	5,887,165	March 23, 1999	Martel et al.			
	5,892,962	April 6, 1999	Cloutier	.		
	5,926,638	July 1999	Inoue			
	5,960,200	September 1999	Eager et al.			
	5,970,254	October 19, 1999	Cooke et al.			
	5,978,260	November 2, 1999	Trimberger et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	6,003,143	December 1999	Kim et al.			
	6,014,509	January 11, 2000	Furtek et al.			
	6,020,758	February 1, 2000	Patel et al.			
	6,021,490	February 1, 2000	Vorbach et al.			
	6,108,760	August 22, 2000	Mirsky et al.			
	6,150,837	November 21, 2000	Beal et al.			
	6,150,839	November 21, 2000	New et al.			
	6,170,051	January 2001	Dowling			
	6,211,697	April 2001	Lien et al.			
	6,212,650	April 2001	Guccione			
	6,240,502	May 29, 2001	Panwar et al.			.
	6,282,701	August 2001	Wygodny et al.			
	6,286,134	September 2001	Click, Jr. et al.			
	6,301,706	October 2001	Maslennikov et al.			
	6,398,383	June 2002	Huang			
	6,404,224	June 11, 2002	Azegami et al.			
	6,421,809	July 2002	Wuytack et al.			
	6,425,068	July 23, 2002	Vorbach			
	6,434,695	August 2002	Esfahani et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,437,441	August 2002	Yamamoto			
	6,490,695	December 2002	Zagorski et al.			
	6,496,971	December 2002	Lesea et al.			

	INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/85		Serial No. 10/791,501		

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. **2885/85** / Serial No. **10/791,501**
	Applicant(s) **Vorbach et al.**
	Filing Date **March 1, 2004** / Group Art Unit **2116**

	6,504,398	January 2003	Lien et al.			
	6,526,520	February 25, 2003	Vorbach et al.			
	6,721,830	April 2004	Vorbach et al.			
	6,961,924	November 2005	Bates et al.			
	2002/0138716	September 26, 2002	Paul et al.			
	2003/0056085	March 2, 2003	Vorbach			
	2003/0014743	January 16, 2003	Cooke et al.			
	2003/0046607	March 6, 2003	Vorbach .			
	2003/0052711	March 20, 2003	Taylor			
	2003/0055861	March 20, 2003	Lai et al.			
	2003/0056091	March 20, 2003	Greenberg			
	2003/0056202	March 20, 2003	Vorbach			
	2003/0093662	May 15, 2003	Vorbach et al.			
	2003/0097513	May 22, 2003	Vorbach et al.			
	2004/0199688	October 2004	Vorbach et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	WO 02/071196	September 12, 2002	PCT				
'	0 463 721	January 2, 1992	EPO				
	0 539 595	May 5, 1993	EPO				
	0 696 001	December 5, 2001	EPO				
	9-27745	January 28, 1997	Japan			Abstract	
	11-307725	November 5, 1999	Japan			Abstract & Partial Translation	
	2000-181566	June 30, 2000	Japan			Computer Translation	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous, A., et al., "The Pleiades Architecture," Chapter I of *The Application of Programmable DSPs in Mobile Communications*, A. Gatherer and A. Auslander, Ed., Wiley, 2002, pp. 1-33.
	Chen et al., "A reconfigurable multiprocessor IC for rapid prototyping of algorithmic-specific high-speed DSP data paths," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, December 1992, pp.1895-1904.
	Hartstein, R., "Coarse grain reconfigurable architectures," Design Automation Conference, 2001, Proceedings of the ASP-DAC 2001 Asia and South Pacific, January 30- February 2, 2001, IEEE 30 January 2001, pp. 564-569.
	Hastie et al., "The implementation of hardware subroutines on field programmable gate arrays," Custom Integrated Circuits Conference, 1990, Proceedings of the IEEE 1990, May 16, 1990, pp. 31.3.1 – 31.4.3 (3 pages).
	John, L., et al., "A Dynamically Reconfigurable Interconnect for Array Processors," Vol. 6, No. 1, March 1998, IEEE, pages 150-157.

		INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/85	Serial No. 10/791,501

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449

Attorney Docket No.	Serial No.
2885/85	10/791,501

Applicant(s)
Vorbach et al.

Filing Date	Group Art Unit
March 1, 2004	2116

	Kastrup, B., "Automatic Hardware Synthesis for a Hybrid Reconfigurable CPU Featuring Philips CPLDs," Proceedings of the PACT Workshop on Reconfigurable Computing, 1998, pp. 5-10.
	Koren et al., "A data-driven VLSI array for arbitrary algorithms," IEEE Computer Society, Long Beach, CA Vol. 21, No. 10, 1 October 1988, pp. 30-34.
	Razdan et al., "A High-Performance Microarchitecture with Hardware-Programmable Functional Units, Micro-27, Proceedings of the 27th Annual International Symposium on Microarchitecture, IEEE Computer Society and Association for Computing Machinery, November 30-December 2, 1994, pp. 172-180.
	Skokan, Z.E., "Programmable logic machine (A programmable cell array)," IEEE Journal of Solid-State Circuits, Vol. 18, Issue 5, October 1983, pp. 572-578.
	Sueyoshi, T, "Present Status and Problems of the Reconfigurable Computing Systems Toward the Computer Evolution," Department of Artificial Intelligence, Kyushi Institute of Technology, Fukuoka, Japan; Institute of Electronics, Information and Communication Engineers, Vol. 96, No. 426, IEICE Technical Report (1996), pp. 111-119 **[English Abstract Only]**
	Siemers et al., "The .>S<puter: A Novel Micoarchitecture Mode for Execution inside Superscalar and VLIW Processors Using Reconfigurable Hardware," Australian Computer Science Communications, Volume 20, No. 4, Computer Architecture, Proceedings of the 3rd Australian Computer Architecture Conference, Perth, John Morris, Ed., February 2-3, 1998, pp. 169-178.
	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
	Yeung, A. et al., "A data-driven architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, *Proceedings VLSI Signal Processing Workshop, IEEE Press*, pp. 225-234, Napa, October 1992.
	Yeung, A. et al., "A reconfigurable data-driven multiprocessor architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, pp. 169-178, *IEEE* 1993.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.